IN THE CLAIMS

Please amend the claims as follows:

1-8. (Canceled)

9. (Previously Presented) A semiconductor apparatus according to claim 23, wherein

the first and second voltage comparison circuits each have a pair of transistors for load and a pair of transistors for input,

the respective driving abilities of the pair of transistors for load of the respective first and second voltage comparison circuits are set so as to be the same, and

the driving abilities of the pair of transistors for input of the first voltage comparison circuit and the pair of transistors for input of the second voltage comparison circuit corresponding thereto are set so as to differ in accordance with a relationship of magnitudes of the signal level of the first reference signal and the signal level of the second reference signal.

10. (Previously Presented) A semiconductor apparatus according to claim 24, wherein

the first and second current comparison circuits each have a pair of transistors for load and a pair of transistors for input,

the respective driving abilities of the pair of transistors for load of the respective first and second current comparison circuits are set so as to be the same, and

the driving abilities of the pair of transistors for input of the first current comparison circuit and the pair of transistors for input of the second current comparison circuit corresponding thereto are set so as to differ in accordance with a relationship of magnitudes

of the signal level of the first reference signal and the signal level of the second reference signal.

11. (Original) A semiconductor apparatus according to claim 9, wherein

the signal level of the first reference signal is greater than the signal level of the second reference signal,

among the pair of transistors for input of the first voltage comparison circuit, the driving ability of the transistor at which the first reference signal is input to a gate thereof is M1, and the driving ability of the transistor at which the input signal is input to a gate thereof is M2, and

among the pair of transistors for input of the second voltage comparison circuit, the driving ability of the transistor at which the input signal is input to a gate thereof is M3, and the driving ability of the transistor at which the second reference signal is input to a gate thereof is M4,

a relationship $M1 > M2 = M3 > M4$ is established among the driving forces M1 to M4.

12. (Original) A semiconductor apparatus according to claim 9, wherein

the signal level of the second reference signal is greater than the signal level of the first reference signal,

among the pair of transistors for input of the first voltage comparison circuit, the driving ability of the transistor at which the first reference signal is input to a gate thereof is M1, and the driving ability of the transistor at which the input signal is input to a gate thereof is M2, and

among the pair of transistors for input of the second voltage comparison circuit, the driving ability of the transistor at which the input signal is input to a gate thereof is M3, and the driving ability of the transistor at which the second reference signal is input to a gate thereof is M4,

a relationship M4 > M2 = M3 > M1 is established among the driving forces M1 to M4.

13. (Original) A semiconductor apparatus according to claim 10, wherein

the signal level of the first reference signal is greater than the signal level of the second reference signal,

among the pair of transistors for input of the first current comparison circuit, the driving ability of the transistor at which current corresponding to the current of the input signal flows is M2, and the driving ability of the transistor at which current corresponding to the current of the first reference signal flows is M3, and

among the pair of transistors for input of the second current comparison circuit, the driving ability of the transistor at which current corresponding to the current of the second reference signal flows is M6, and the driving ability of the transistor at which current corresponding to the current of the input signal flows is M7,

a relationship M3 > M2 = M7 > M6 is established among the driving forces M2, M3, M6, and M7.

14. (Original) A semiconductor apparatus according to claim 10, wherein

the signal level of the second reference signal is greater than the signal level of the first reference signal, and

among the pair of transistors for input of the first current comparison circuit, the driving ability of the transistor at which current corresponding to the current of the input signal flows is M2, and the driving ability of the transistor at which current corresponding to the current of the first reference signal flows is M3, and

among the pair of transistors for input of the second current comparison circuit, the driving ability of the transistor at which current corresponding to the current of the second reference signal flows is M6, and the driving ability of the transistor at which current corresponding to the current of the input signal flows is M7,

a relationship M6 > M2 = M7 > M5 is established among the driving forces M2, M3, M6, and M7.

15-22. (Canceled)

23. (Previously Presented) A semiconductor apparatus having a logic level decision circuit, the logic level decision circuit comprising:

a first comparison circuit which compares an input signal with a first reference signal corresponding to logic "1" level, and which outputs a first differential signal;

a second comparison circuit which compares the input signal with a second reference signal corresponding to logic "0" level, and which outputs a second differential signal; and

a third comparison circuit which compares the output of the first comparison circuit and the output of the second comparison circuit, and which decides a logic level of the input signal,

wherein the logic level decision circuit is a voltage input type logic level decision circuit; and

the first comparison circuit is a current mirror type first voltage comparison circuit, and the second comparison circuit is a current mirror type second voltage comparison circuit.

24. (Previously Presented) A semiconductor apparatus having a logic level decision circuit, the logic level decision circuit comprising:

a first comparison circuit which compares an input signal with a first reference signal corresponding to logic "1" level, and which outputs a first differential signal;

a second comparison circuit which compares the input signal with a second reference signal corresponding to logic "0" level, and which outputs a second differential signal; and

a third comparison circuit which compares the output of the first comparison circuit and the output of the second comparison circuit, and which decides a logic level of the input signal,

wherein the logic level decision circuit is a current input type logic level decision circuit; and

the first comparison circuit is a current mirror type first current comparison circuit, and the second comparison circuit is a current mirror type second current comparison circuit.